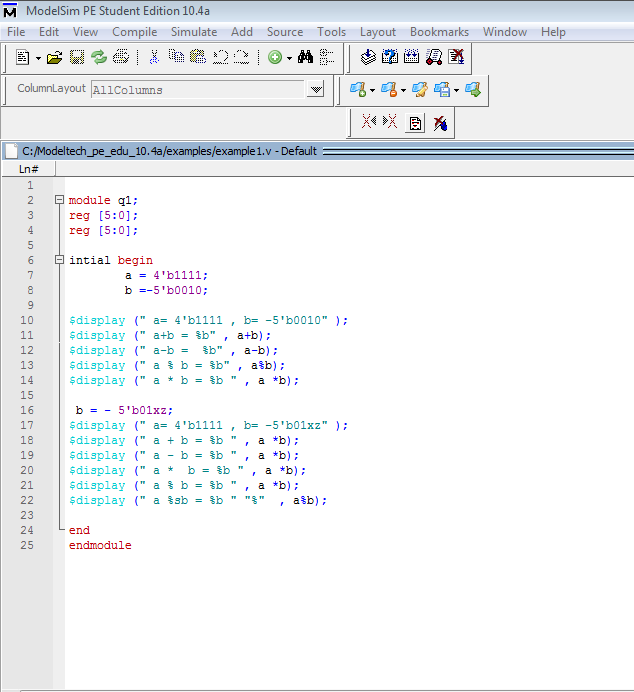
Chirag solanki

15035

Lab assignment 2

Answers 1



module q1;

reg [5:0];

reg [5:0];

intial begin

a = 4'b1111;

b =-5'b0010;

$display (" a= 4'b1111 , b= -5'b0010" );

$display (" a+b = %b" , a+b);

$display (" a-b = %b" , a-b);

$display (" a % b = %b" , a%b);

$display (" a \* b = %b " , a \*b);

b = - 5'b01xz;

$display (" a= 4'b1111 , b= -5'b01xz" );

$display (" a + b = %b " , a \*b);

$display (" a - b = %b " , a \*b);

$display (" a \* b = %b " , a \*b);

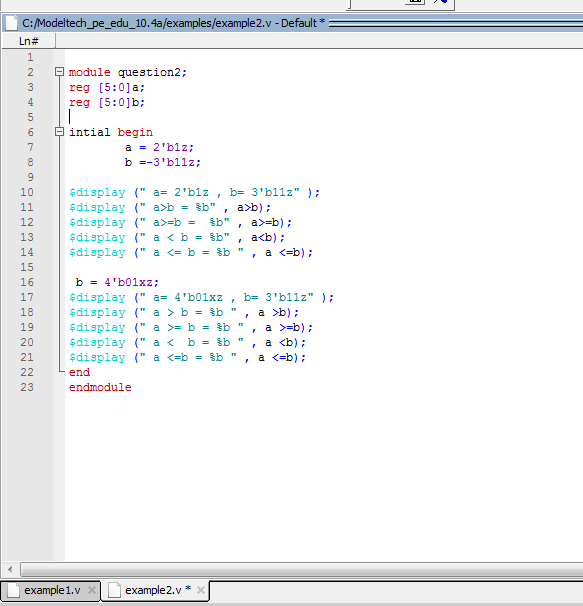
$display (" a % b = %b " , a \*b);

$display (" a %sb = %b " "%" , a%b);

end

endmodule

Answer 2



module question2;

reg [5:0]a;

reg [5:0]b;

intial begin

a = 2'b1z;

b =-3'b11z;

$display (" a= 2'b1z , b= 3'b11z" );

$display (" a>b = %b" , a>b);

$display (" a>=b = %b" , a>=b);

$display (" a < b = %b" , a<b);

$display (" a <= b = %b " , a <=b);

b = 4'b01xz;

$display (" a= 4'b01xz , b= 3'b11z" );

$display (" a > b = %b " , a >b);

$display (" a >= b = %b " , a >=b);

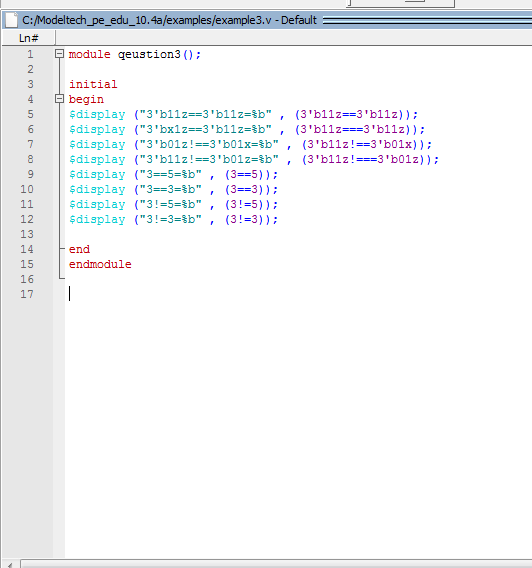
$display (" a < b = %b " , a <b);

$display (" a <=b = %b " , a <=b);

end

endmodule

Answers 3



module qeustion3();

initial

begin

$display ("3'b11z==3'b11z=%b" , (3'b11z==3'b11z));

$display ("3'bx1z==3'b11z=%b" , (3'b11z===3'b11z));

$display ("3'b01z!==3'b01x=%b" , (3'b11z!==3'b01x));

$display ("3'b11z!==3'b01z=%b" , (3'b11z!===3'b01z));

$display ("3==5=%b" , (3==5));

$display ("3==3=%b" , (3==3));

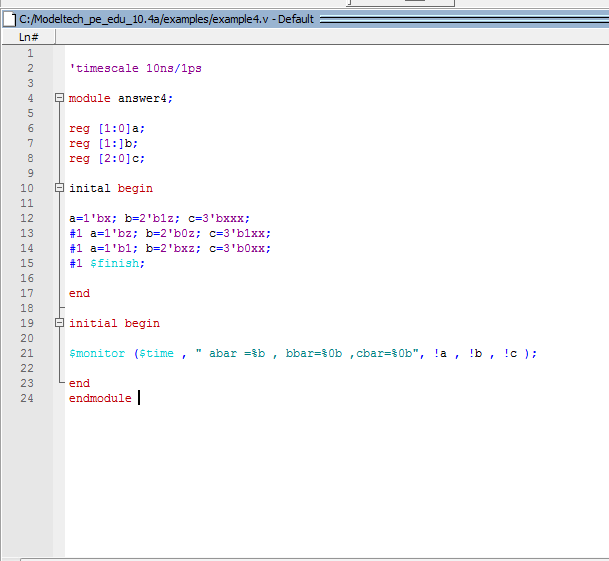
$display ("3!=5=%b" , (3!=5));

$display ("3!=3=%b" , (3!=3));

end

endmodule

example 4



'timescale 10ns/1ps

module answer4;

reg [1:0]a;

reg [1:]b;

reg [2:0]c;

inital begin

a=1'bx; b=2'b1z; c=3'bxxx;

#1 a=1'bz; b=2'b0z; c=3'b1xx;

#1 a=1'b1; b=2'bxz; c=3'b0xx;

#1 $finish;

end

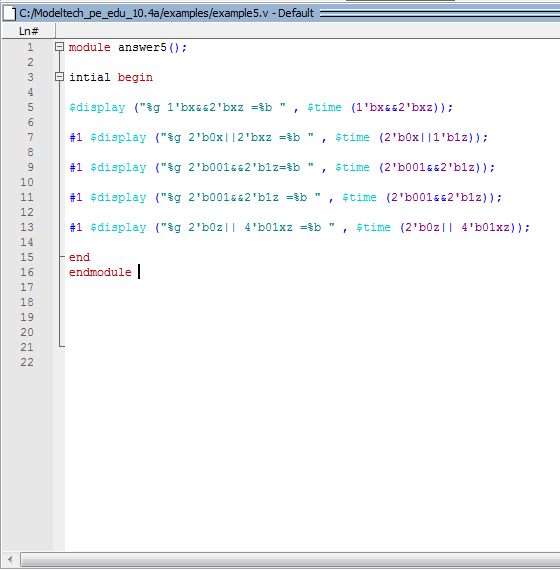
initial begin

$monitor ($time , " abar =%b , bbar=%0b ,cbar=%0b", !a , !b , !c );

end

endmodule

example 5



module answer5();

intial begin

$display ("%g 1'bx&&2'bxz =%b " , $time (1'bx&&2'bxz));

#1 $display ("%g 2'b0x||2'bxz =%b " , $time (2'b0x||1'b1z));

#1 $display ("%g 2'b001&&2'b1z=%b " , $time (2'b001&&2'b1z));

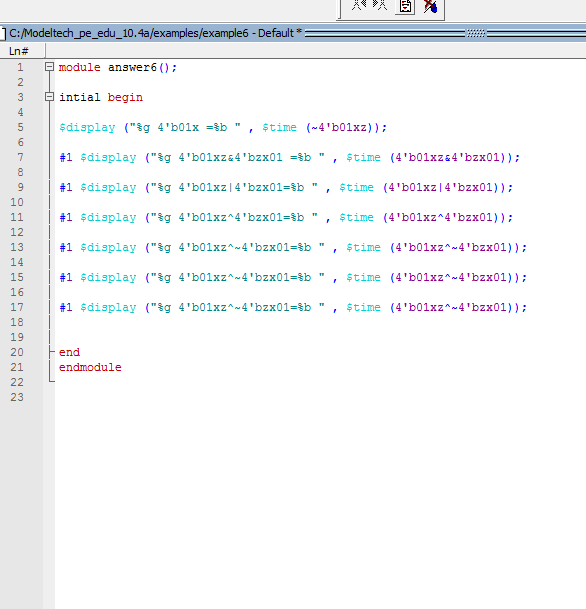
#1 $display ("%g 2'b001&&2'b1z =%b " , $time (2'b001&&2'b1z));

#1 $display ("%g 2'b0z|| 4'b01xz =%b " , $time (2'b0z|| 4'b01xz));

end

endmodule

answer 6



module answer6();

intial begin

$display ("%g 4'b01x =%b " , $time (~4'b01xz));

#1 $display ("%g 4'b01xz&4'bzx01 =%b " , $time (4'b01xz&4'bzx01));

#1 $display ("%g 4'b01xz|4'bzx01=%b " , $time (4'b01xz|4'bzx01));

#1 $display ("%g 4'b01xz^4'bzx01=%b " , $time (4'b01xz^4'bzx01));

#1 $display ("%g 4'b01xz^~4'bzx01=%b " , $time (4'b01xz^~4'bzx01));

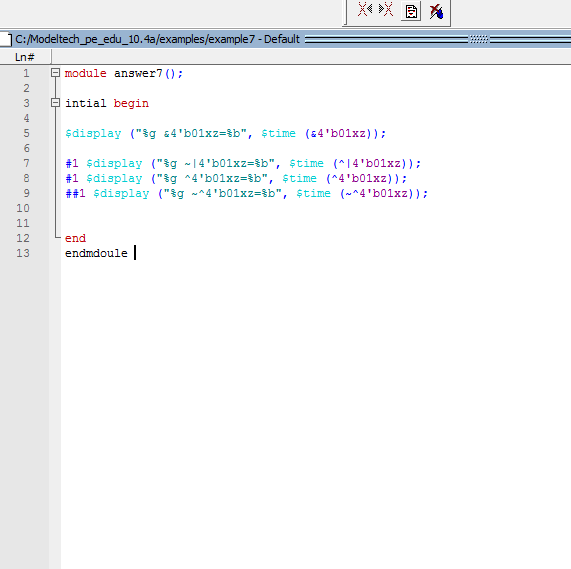
#1 $display ("%g 4'b01xz^~4'bzx01=%b " , $time (4'b01xz^~4'bzx01));

#1 $display ("%g 4'b01xz^~4'bzx01=%b " , $time (4'b01xz^~4'bzx01));

end

endmodule

answer 7



module answer7();

intial begin

$display ("%g &4'b01xz=%b", $time (&4'b01xz));

#1 $display ("%g ~|4'b01xz=%b", $time (^|4'b01xz));

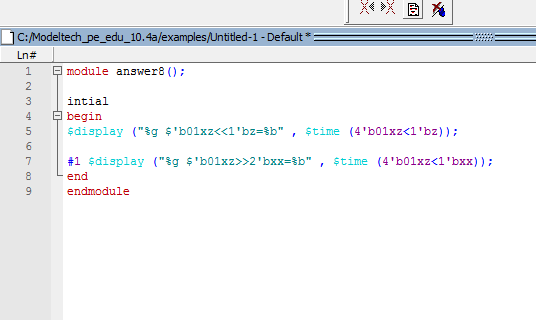
#1 $display ("%g ^4'b01xz=%b", $time (^4'b01xz));

##1 $display ("%g ~^4'b01xz=%b", $time (~^4'b01xz));

end

endmdoule

answer 8



module answer8();

intial

begin

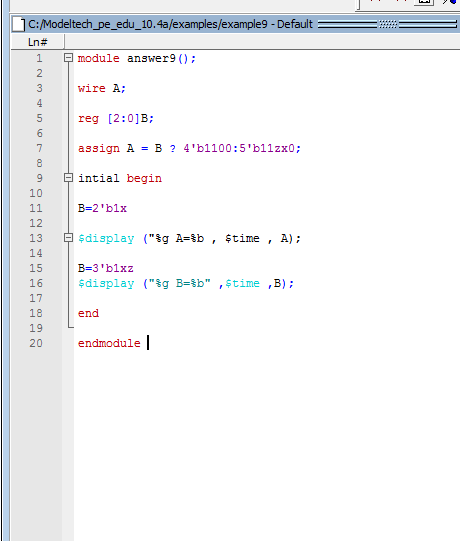
$display ("%g $'b01xz<<1'bz=%b" , $time (4'b01xz<1'bz));

#1 $display ("%g $'b01xz>>2'bxx=%b" , $time (4'b01xz<1'bxx));

end

endmodule

example 9



module answer9();

wire A;

reg [2:0]B;

assign A = B ? 4'b1100:5'b11zx0;

intial begin

B=2'b1x

$display ("%g A=%b , $time , A);

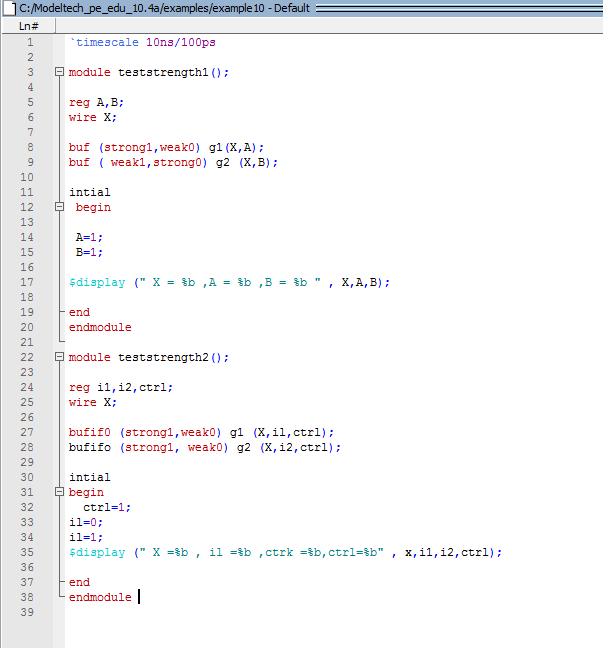
B=3'b1xz

$display ("%g B=%b" ,$time ,B);

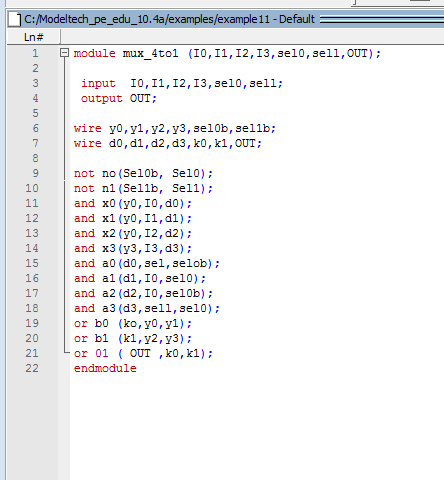
end

endmodule

example 10



Example 11



module mux\_4to1 (I0,I1,I2,I3,sel0,sell,OUT);

input I0,I1,I2,I3,sel0,sell;

output OUT;

wire y0,y1,y2,y3,sel0b,sel1b;

wire d0,d1,d2,d3,k0,k1,OUT;

not no(Sel0b, Sel0);

not n1(Sel1b, Sel1);

and x0(y0,I0,d0);

and x1(y0,I1,d1);

and x2(y0,I2,d2);

and x3(y3,I3,d3);

and a0(d0,sel,selob);

and a1(d1,I0,sel0);

and a2(d2,I0,sel0b);

and a3(d3,sell,sel0);

or b0 (ko,y0,y1);

or b1 (k1,y2,y3);

or 01 ( OUT ,k0,k1);

endmodule

`timescale 10ns/100ps

module teststrength1();

reg A,B;

wire X;

buf (strong1,weak0) g1(X,A);

buf ( weak1,strong0) g2 (X,B);

intial

begin

A=1;

B=1;

$display (" X = %b ,A = %b ,B = %b " , X,A,B);

end

endmodule

module teststrength2();

reg i1,i2,ctrl;

wire X;

bufif0 (strong1,weak0) g1 (X,il,ctrl);

bufifo (strong1, weak0) g2 (X,i2,ctrl);

intial

begin

ctrl=1;

il=0;

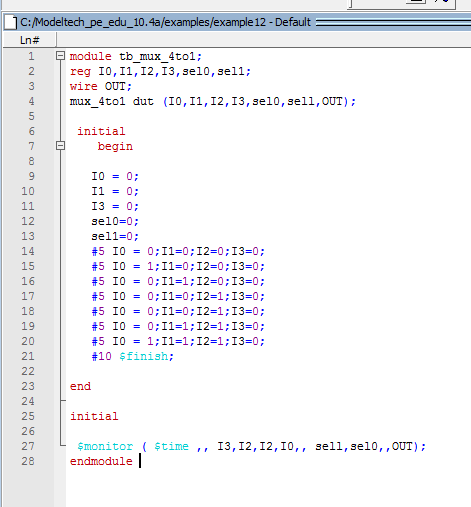
il=1;

$display (" X =%b , il =%b ,ctrk =%b,ctrl=%b" , x,i1,i2,ctrl);

end

endmodule

example 12



module tb\_mux\_4to1;

reg I0,I1,I2,I3,sel0,sel1;

wire OUT;

mux\_4to1 dut (I0,I1,I2,I3,sel0,sell,OUT);

initial

begin

I0 = 0;

I1 = 0;

I3 = 0;

sel0=0;

sel1=0;

#5 I0 = 0;I1=0;I2=0;I3=0;

#5 I0 = 1;I1=0;I2=0;I3=0;

#5 I0 = 0;I1=1;I2=0;I3=0;

#5 I0 = 0;I1=0;I2=1;I3=0;

#5 I0 = 0;I1=0;I2=1;I3=0;

#5 I0 = 0;I1=1;I2=1;I3=0;

#5 I0 = 1;I1=1;I2=1;I3=0;

#10 $finish;

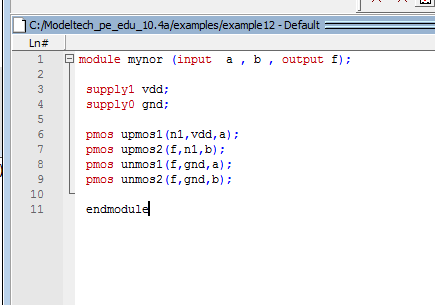
end

initial

$monitor ( $time ,, I3,I2,I2,I0,, sell,sel0,,OUT);

endmodule

example 12



module mynor (input a , b , output f);

supply1 vdd;

supply0 gnd;

pmos upmos1(n1,vdd,a);

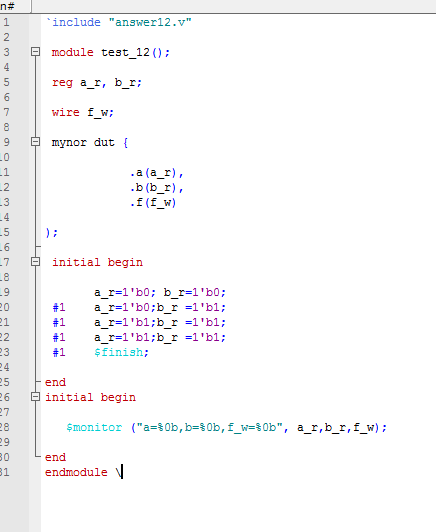
pmos upmos2(f,n1,b);

pmos unmos1(f,gnd,a);

pmos unmos2(f,gnd,b);

endmodule

test batch :



`include "answer12.v"

module test\_12();

reg a\_r, b\_r;

wire f\_w;

mynor dut {

.a(a\_r),

.b(b\_r),

.f(f\_w)

);

initial begin

a\_r=1'b0; b\_r=1'b0;

#1 a\_r=1'b0;b\_r =1'b1;

#1 a\_r=1'b1;b\_r =1'b1;

#1 a\_r=1'b1;b\_r =1'b1;

#1 $finish;

end

initial begin

$monitor ("a=%0b,b=%0b,f\_w=%0b", a\_r,b\_r,f\_w);

end

endmodule \